Fan/Motor Pre-Drivers

FEATURES

- **Variable speed control for 4-wire fans**
- **Separate Tach and Alarm Pins**
- **Soft switching to reduce audible noise (AGV8012)**
- **Current limit protection**
- **Locked rotor detect and auto-retry**
- **Integrated Hall amplifier**
- **Interfaces with standard digital temp sensors**
- **Available in a narrow 14 lead SOIC RoHS=compliant package**

APPLICATIONS

- **PCs, workstations, servers**
- **Industrial fans and blowers**

DESCRIPTION

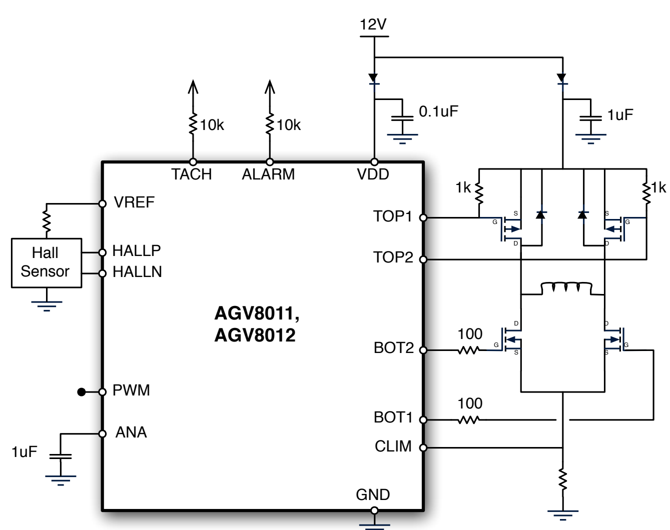
The AGV8011 and AGV8012 are single phase brushless DC fan/motor pre-drivers suitable for 4-wire fan applications.

Variable speed is adjusted by varying the duty cycle to the PWM control input pin. The analog control pin can be used to interface with a thermistor when the PWM input control is not needed.

Both pre-drivers have separate Tach and Alarm pins. Current limit, locked rotor and thermal protections are also provided. The 40V MOS output predrivers can source or sink 100mA.

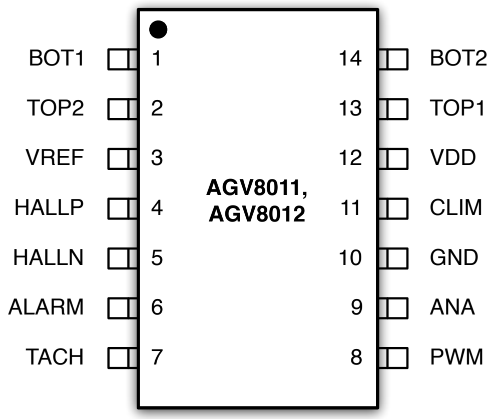
In addition, the AGV8012 provides soft switching to reduce audible noise.

TYPICAL APPLICATION



PIN CONFIGURATION

14-Lead SOIC



ORDERING INFORMATION

Part Number	Package[1,2]	Quantity per Reel	Package Marking[3]
AGV8011S-T1	SOIC14	1,000	AGV8011 Ayww
AGV8011S-T2	SOIC14	2,000	AGV8011 Ayww
AGV8012S-T1	SOIC14	1,000	AGV8012 Ayww
AGV8012S-T2	SOIC14	2,000	AGV8012 Ayww

Notes: 1. Matte-Tin Plated Finish (RoHS-compliant)
2. Narrow body SOIC package.
3. Ayww - Assembly site, year, work week.

ABSOLUTE MAXIMUM RATINGS

(V_{DD}=12V, T_A=25°C unless otherwise specified)

Parameter	Symbol	Rating	Units
Supply voltage (pin 12)	V_{DD}	20	V
Top drive outputs (pins 2, 13) Voltage Sink current	 V_{TOP} $I_{SINK,TOP}$	 -0.3 to 40 100	 V mA
Bottom drive outputs (pins 1, 14) Source and sink current	 I_{BOT}	 100	 mA
TACH, Alarm (pins 7, 6) Voltage Sink current	 V_{TACH} $I_{SINK,TACH}$	 -0.3 to 40 10	 V mA
3.3V Reference output current (pin3)	I_{REF}	internally limited	mA
Hall inputs (pins 4, 5)	V_{HALL}	-0.3 to V_{DD}	V
Minimum RPM input (pin 6)	V_{MIN}	-0.3 to 7	V
PWM Control input (pin 8)	V_{PWM}	-0.3 to 7	V
Analog control input (pin 9)	V_{ANA}	-0.3 to 7	V
Current limit sense (pin11)	V_{CLIM}	-0.3 to 7	V
Operating junction temperature[1]	T_J	-40 to 150	°C
Storage temperature	T_{STG}	-60 to 150	°C
IR reflow peak temperature	T_{REFLOW}	220	°C
Lead soldering temperature (10 seconds)	T_{LEAD}	300	°C
Electrostatic discharge Human body model[2] Machine Model[3]	 $V_{ESD,HBM}$ $V_{ESD,MM}$	 2000 250	 V V

Notes:

1. Package power dissipation limits must be observed. Thermal resistance junction to air SOIC-14 package $R_{\Theta JA}$=120°C/W
2. Human body model: 100pF capacitor discharged through 1.5kΩ into pin.
3. Machine model: 200pF capacitor discharged directly into pin.

RECOMMENDED OPERATING CONDITIONS

(V_{DD}=12V, T_A=25°C unless otherwise specified)

Parameter	Symbol	Range	Units
Supply voltage (pin 12)	V_{DD}	5.5 to 16	V
Top drive output voltage (pins 2, 13)	V_{TOP}	0 to 40	V
TACH, Alarm (pins 7, 6)	V_{TACH}	0 to V_{DD}	V
3.3V Reference Loading	I_{REF}	0 to 10	mA
Hall inputs (pins 4, 5)	V_{HALL}	0 to V_{REF}	V
Minimum RPM input (pin 6)	V_{MIN}	0 to V_{REF}	V
PWM Control input (pin 8, internal 10kΩ pullup)	V_{PWM}	0 to V_{REF}	V
Analog control input (pin 9)	V_{ANA}	0 to V_{REF}	V
Current limit sense (pin11)	V_{CLIM}	0 to 200	mV
Ambient temperature	T_J	-40 to 85	°C

ELECTRICAL OPERATING CHARACTERISTICS

(V_{DD}=12V, T_A=25°, over recommended operating conditions unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Top Side Pre-Driver Outputs						
Low State Voltage	$V_{LOW,TOP}$	I_{SINK}=0mA	-	0	-	V
		I_{SINK}=50mA	-	0.5	-	
High State Leakage Current	$I_{LEAK,TOP}$	V_{TOP}=40V	-	-	1.0	µA
Fall Time	$t_{F,TOP}$	R_{PULLUP}=1kΩ, C_{LOAD}=1nF	-	105	-	nS
Bottom Side Pre-Driver Outputs						
Low State Voltage	$V_{LOW,BOT}$	I_{SINK}=0mA	-	0	-	V
		I_{SINK}=50mA	-	1.2	-	V
High State Voltage	$V_{HIGH,BOT}$	I_{SOURCE}=0mA,V_{DD}=12V	-	12	-	V
		I_{SOURCE}=50mA,V_{DD}=12V	-	10.6	-	V
High State Leakage Current	$I_{LEAK,BOT}$	V_{TOP}=16V	-	-	1.0	µA
Rise and Fall Times	$t_{R,BOT}$	C_{LOAD}=1nF	-	80	-	nS
	$t_{F,BOT}$	C_{LOAD}=1nF	-	85	-	nS
TACH, ALARM						
Low State Voltage	$V_{LOW,TACH}$	I_{SINK}=1.2mA (R_{PULLUP}=10kΩ,V_{DD}=12V)	-	0.2	-	V
High State Leakage Current	$I_{LEAK,TACH}$	V_{TACH}=16V	-	-	1.0	µA
Fall Time	$t_{F,TACH}$	R_{PULLUP}=10kΩ, C_{LOAD}=100pF	-	95	-	nS
3.3V Reference						
Output Voltage	V_{REF}	I_O=5mA	3.135	3.3	3.465	V
Load Regulation	REG_{LOAD}	I_O=0mA to 10mA	-	1.0	30	mV
Line Regulation	REG_{LINE}	V_{DD}=6V to 15V, I_O=5mA	-	2.0	30	mV
Short Circuit Current	I_{SC}		-	27	-	mA
Hall Amplifier						
Common Mode Voltage Range	$V_{CM,HALL}$		-	-0.2 to 3.3	-	V
Input Hysteresis Trip Points	$V_{TRIP,HALL}$	V_{CM}=300mV	-	$V_{CM}\mp17$	-	mV
Maximum Input Frequency	$f_{MAX,HALL}$		-	4	-	kHz
Current Limit						
Threshold Voltage	$V_{TH,CLIM}$	V_{CLIM} increasing	180	200	220	mV
Hysteresis	$V_{HYS,CLIM}$		-	20	-	mV
Bottom Drive Turn Off Propagation Delay	$t_{OFF,CLIM}$	$V_{TH,CLIM}$ overdrive=10%	-	200	-	nS
PWM Control						
Threshold Voltage	$V_{TH,PWM}$	V_{PWM} increasing	-	1.65	-	V
Hysteresis	$V_{HYS,PWM}$		-	70	-	mV
Pull Up Voltage	$V_{UP,PWM}$		-	3.3	-	V
Pull Up Resistance	$R_{UP,PWM}$		-	10	-	kΩ
Analog Control						
0% of Max RPM Voltage Level	$V_{LOW,ANA}$		0.95	1.0	1.05	V
100% of Max RPM Voltage Level	$V_{HI,ANA}$		2.85	3.0	3.15	V
Integrating Input Resistance			-	1.0	-	MΩ

Closed Loop Maximum RPM						
Steady State Closed Loop Speed		worst case part to part variation for properly designed system	-1	-	+1	%
Pulse Width Modulation						
Bottom Drive PWM frequency	f_{PWM}		-	30	-	kHz
Commutation Non-Overlap Delay	t_{COM}		-	70	-	µS
Fault Retry Timer						
Minimum Hall Frequency without Fault Detect	f_{FAULT}	50% duty cycle	-	1	-	Hz
Cool Down Duration	t_{COOL}		-	8	-	S
Retry Duration	t_{RETRY}		-	0.5	-	S
Under Voltage Shutdown						
Supply Voltage Required to Enable Bottom Drivers	$V_{TH,UV}$	V_{DD} Increasing	-	4.7	-	V
Under Voltage Hysteresis	$V_{HYS,UV}$		-	500	-	mV
Thermal Shutdown						
Shutdown Temperature	T_{SD}		-	150	-	°C
Thermal Hysteresis	T_{HYS}		-	15	-	°C
Total Device						
Current Consumption	I_{DD}	V_{REF} Unloaded, No PWM (PWM Control Float High, Analog Control Grounded, Min Speed Grounded)	-	1.4	-	mA

TYPICAL PERFORMANCE CHARACTERISTICS

(Vdd=12V, Ta=25°C unless otherwise specified)

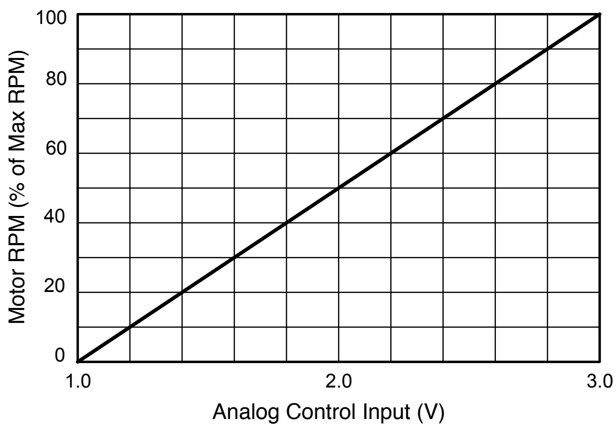


Fig.1: Analog Control

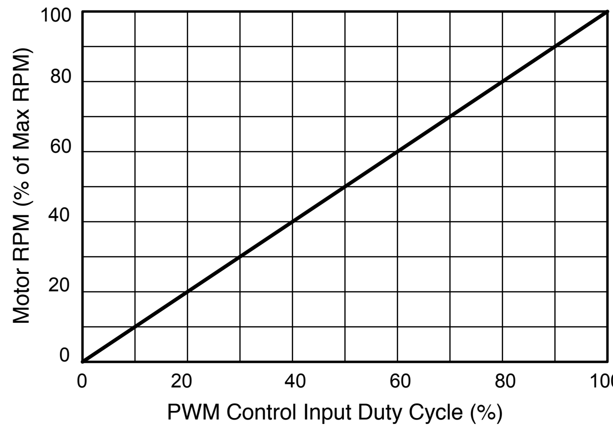


Fig.2: PWM Control

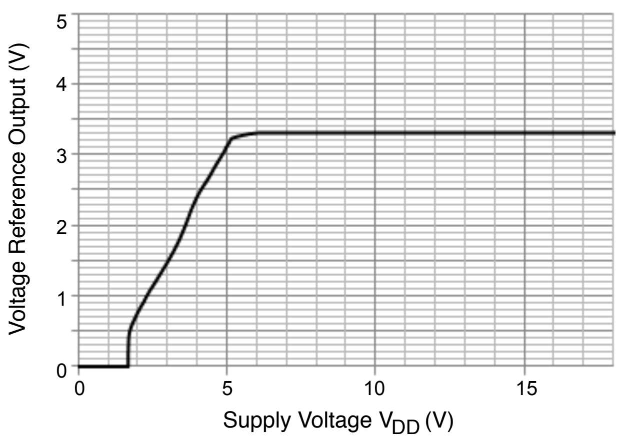


Fig.3: Voltage Reference Versus Supply

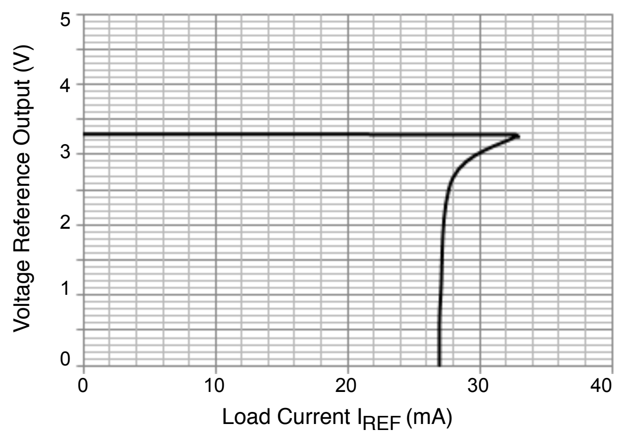


Fig.4: Voltage Reference Versus Load

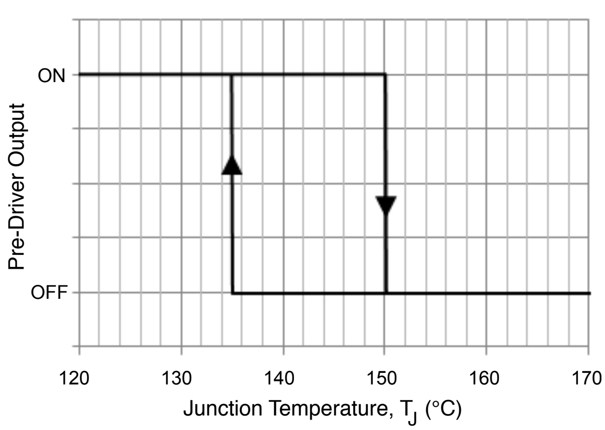


Fig.5: Thermal Shutdown

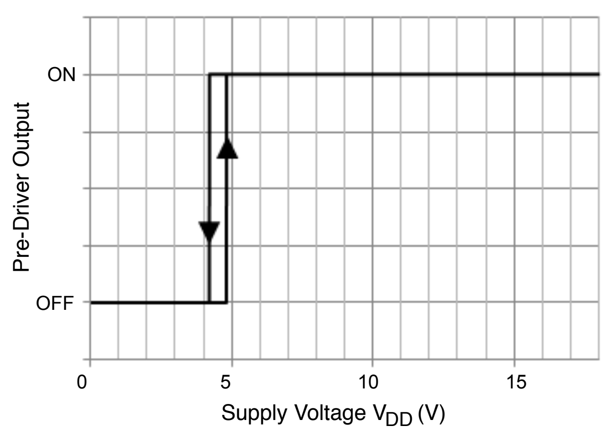


Fig.6: Under Voltage Shutdown

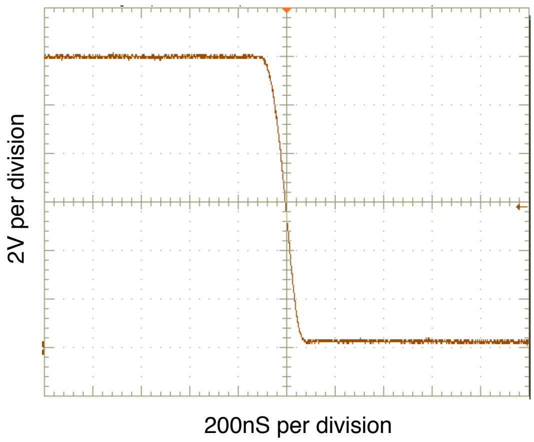


Fig.7: Top Side Pre-Driver (R_{PULLUP}=1kΩ ,C_L=1nF)

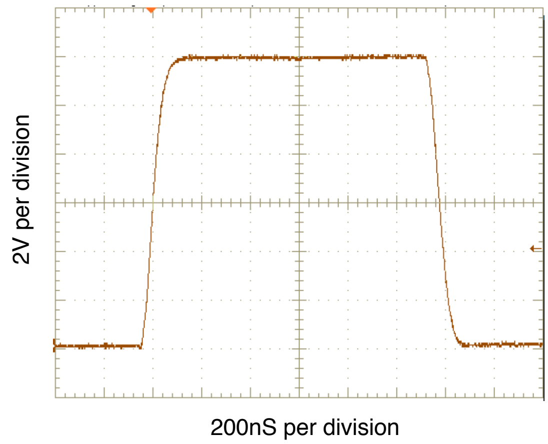


Fig.8: Bottom Side Pre-Driver (R_L=10MΩ ,C_L=1nF)

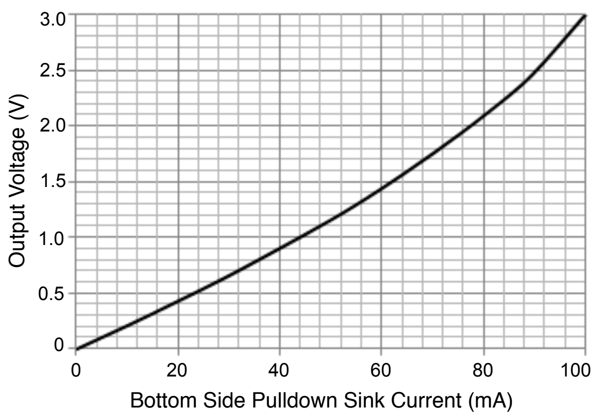


Fig.9: Bottom Side Pre-Driver Pull Down Voltage Versus Sink Current

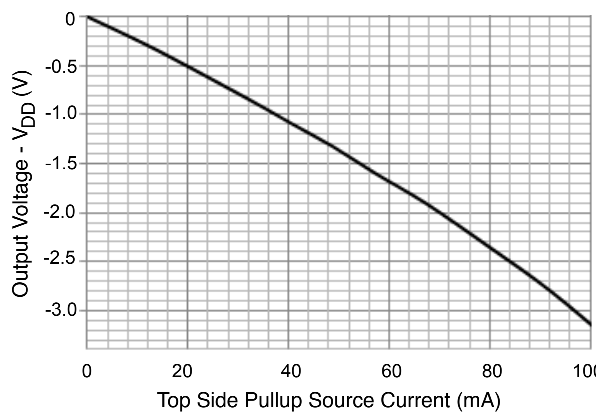


Fig.10: Bottom Side Pre-Driver Pull Up Voltage Versus Source Current (V_{DD}=12V)

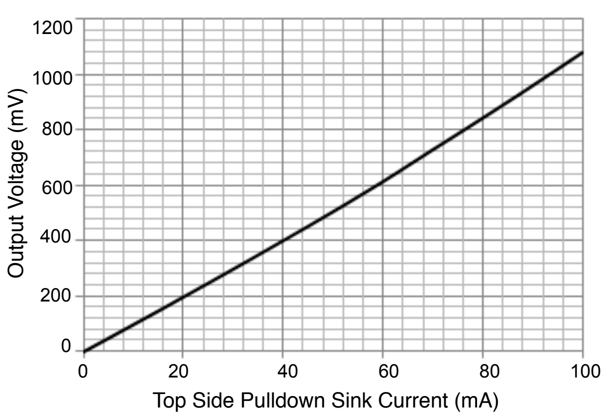


Fig.11: Top Side Pre-Driver Pull Down Voltage Versus Sink Current

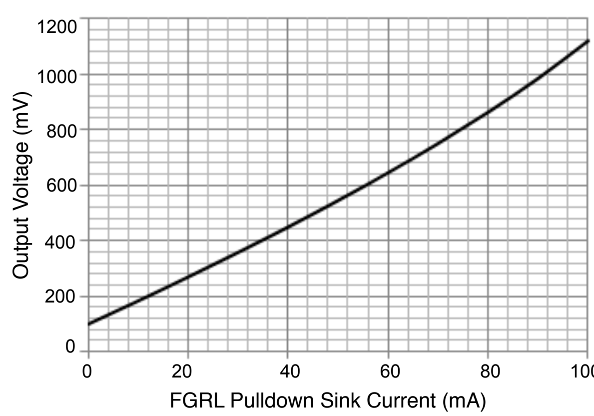


Fig.12: TACH, Alarm Pull Down Voltage Versus Sink Current

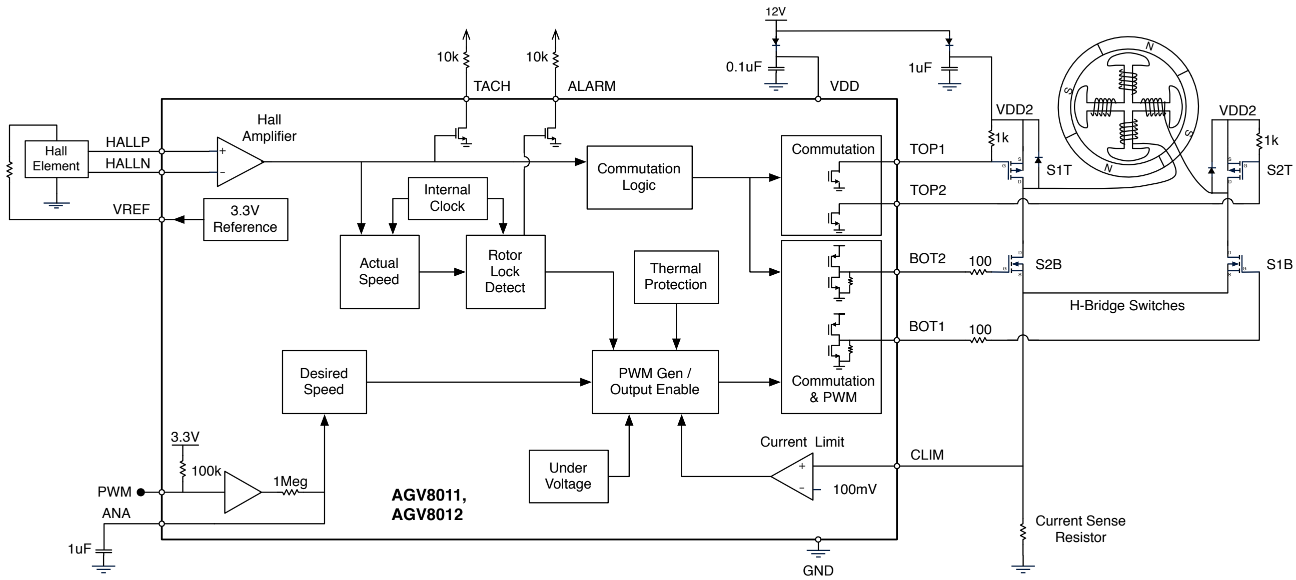


Fig.13: Detailed Block Diagram of Typical Application

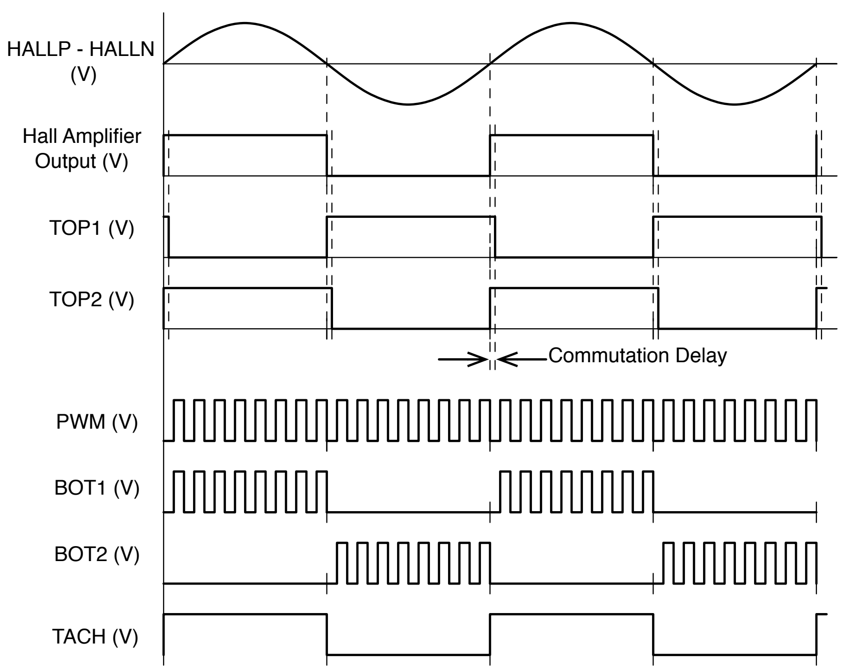


Fig.14: Typical Commutation Waveforms

PIN DESCRIPTION

VDD, GND are the power and ground connections. For best performance a bypass capacitor of at least 0.1μF should be placed between VDD and ground close to the VDD pin.

BOT1, BOT2 are the bottom side pre-driver outputs that connect to the NMOS H-Bridge switches. These high voltage CMOS outputs switch between VDD and ground at the PWM frequency of 30kHz and can source and sink 100mA. Commutation logic determines which of the two bottom side pre-drivers is active. Internal 20kΩ pulldown resistors guarantee the H-Bridge is turned off when power is first applied.

TOP1, TOP2 are the top side pre-driver outputs that connect to the PMOS H-Bridge switches. These high voltage NMOS pulldown switches are 40V tolerant and can sink 100mA. The top drives are not PWMed and only switch at the commutation frequency.

HALLP, HALLN are the differential inputs to the integrated Hall amplifier. The hall amplifier has a common mode range of -0.2V to 3.3V, and differential hysteresis trip points of +/- 17mV.

VREF is a 3.3V regulated voltage reference. VREF should be used to bias the MIN and MAX RPM pins and can be used to bias the Hall Effect sensor. Fold-back current limiting limits the short circuit current to below 30mA.

MIN sets the minimum open loop RPM of the motor. Biasing MIN from 1V to 3V programs the minimum speed from 0% to 100% of MAX RPM.

ANA is the analog control input. Biasing ANA from 1V to 3V programs the steady state closed loop speed from 0% to 100% of MAX RPM. If the voltage on ANA falls below the voltage on MIN, then MIN sets the closed loop speed.

PWM This control input converts the incoming PWM duty cycle to an analog voltage on the ANA pin. An internal 10kΩ resistor pulls an open drain input up to 3.3V. When this input is used, an integrating capacitor should be placed between ANA and ground. Varying the duty cycle on PWM from 0% to 100% adjusts the closed loop steady state RPM from 0% to 100% of MAX RPM.

CLIM is the current limit input. The bottom side pre-drivers are disabled if the voltage on CLIM exceeds 200mV. The current limit comparator has 20mV of hysteresis. The pre-drivers will be enabled again after the next PWM cycle when CLIM falls below 180mV.

TACH Tach is an open drain output that transitions between a logical 1 and 0 as inputs to the Hall amplifier change polarity. This open drain output is 40V tolerant.

ALARM Alarm is an open drain output that connects to an external pull up resistor. Rotor lock condition is identified when no activity is detected on Hall amplifier for longer than 0.5 seconds. When this occurs, the alarm pin will go high. This open drain output is 40V tolerant.

BASIC OPERATION

The AGV8011 and AGV8012 are identical parts with the exception that the AGV8012 also provides soft switching to reduce audible noise. Unless stated otherwise within the text, the description of the AGV8012 also applies to the AGV8011. Fig. 13 shows a detailed block diagram of a typical application. A system thermal controller or temperature sensor reports the system temperature to the AGV8012 in the form of a control signal representing the desired speed of the fan. The desired speed control signal can either be a PWM duty cycle applied to the PWM pin or an analog voltage applied to the ANA pin The differential output of the Hall Effect sensor gets amplified by the Hall Amplifier to determine the how the rotor's magnetic poles, north or south, are oriented with respect to the stator. This position information is processed by the Commutation Logic block to choose the direction of current flow in the stator windings. The PWM Generator adjusts the PWM duty cycle that gets applied to the H-Bridge switches in order to set the average voltage across the motor. The timing diagram of Fig. 14 shows typical commutation waveforms. The AGV8012 has a commutation delay (non-overlap delay) of 70µS.

Setting Desired Speed with ANA Pin

The AGV8012 has two separate pins, ANA and PWM, that can be used to adjust fan speed. ANA is the analog control input. When an analog voltage is used to directly drive the ANA pin, PWM should be left to float high, and the capacitor connected to ANA in Fig. 13 is not needed.

Like MIN, the voltage on ANA is also compared internally against VREF. If a thermistor is used to control ANA, biasing the thermistor bridge from VREF will make the desired RPM insensitive to part to part variations in VREF. For the nominal value of VREF=3.3V

$$\text{Desired Speed} = 100 \cdot \frac{\text{ANA - 1V}}{\text{2V}} \quad \text{\% of MAX RPM}$$

The desired speed can be adjusted linearly by varying ANA is between 1V and 3V.

$$\text{ANA} = 1\text{V} \quad \Longrightarrow \quad \text{Desired Speed is 0 RPM}$$

$$\text{ANA} = 3\text{V} \quad \Longrightarrow \quad \text{Desired Speed is 100\% of MAX RPM}$$

If the voltage on ANA drops below the value on MIN, then the voltage on MIN will be used to control the fan at the programmed minimum speed. Fig. 1 shows motor RPM versus analog control voltage.

Setting Desired Speed with PWM Pin

The PWM control input converts the incoming PWM duty cycle to an analog voltage on the ANA pin. An internal 10kΩ resistor pulls an open drain input up to 3.3V. When this input is used, an integrating capacitor should be placed between ANA and ground. Fig. 13 shows how the internal 10kΩ pull-up resistor is coupled to the PWM comparator. The comparator's output is internally clamped between 1V and 3V; and connects to the ANA pin via a 1MΩ resistor. With an integrating capacitor placed between ANA and ground, varying the duty cycle on PWM from 0% to 100% linearly adjusts the voltage on ANA between 1V and 3V. This in turn adjusts the desired speed from 0% to 100% of MAX RPM.

$$\text{Desired Speed} = \text{PWM Duty Cycle} \cdot \text{MAX RPM}$$

For duty cycles of 0% and 100%

$$\text{PWM Duty Cycle} = 0\% \quad \Longrightarrow \quad \text{Desired Speed is 0 RPM}$$

$$\text{PWM Duty Cycle} = 100\% \quad \Longrightarrow \quad \text{Desired Speed is 100\% of MAX RPM}$$

If the duty cycle is low enough such that the voltage on ANA drops below the value on MIN, then the voltage on MIN will be used to control the fan at the programmed minimum speed. Fig. 2 shows motor RPM versus PWM control duty cycle.

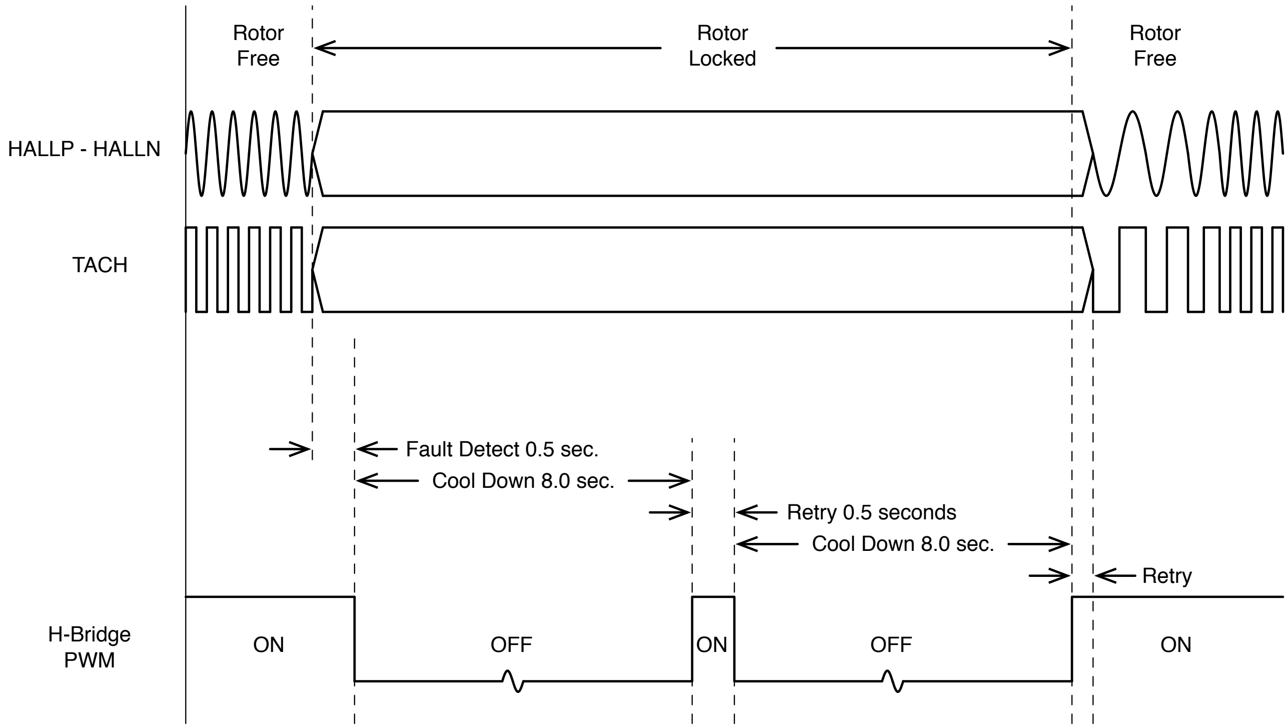


Fig.15: Rotor Lock Detect, Cool Down - Retry, TACH

FAULT PROTECTION FEATURES

Referring back to Fig. 13, the Output Enable block enables the bottom NMOS H-Bridge switches to conduct current only if no fault conditions exist. If a fault condition occurs, the bottom switches in the H-Bridge are turned off, disabling current to the motor windings. Four fault conditions will disable the motor: rotor lock, current limit, thermal overload, and under voltage.

Rotor Lock

Rotor Lock Detect monitors the Hall Amplifier output and uses the internal clock to measure the rotor speed. If the rotor speed falls below a certain threshold, it is assumed there is a blockage stopping the rotor and the motor is disabled before unsafe current levels build up in the windings. Specifically, if the Hall amplifier hasn't detected a change in polarity on the Hall inputs for a duration of 0.5 seconds, then the bottom drives in the H-Bridge are disabled. The bottom drives remain disabled for a Cool Down period of 8 seconds. At which point, the motor goes through a Retry period for 0.5 seconds to determine if the the locked rotor condition still persists. If the rotor fails to turn during Retry, then the Cool Down - Retry cycle will repeat as long as the motor is being commanded to run. If however, the Hall Amplifier detects that the rotor has moved during the retry period, then normal operation will resume (see Fig. 15).

Thermal Protection

The AGV8012 has its own thermal sensor inside the Thermal Protection block. As the controller IC is typically located inside the fan, the IC temperature is an indication of the fan. If the IC gets too hot, the motor is disabled. Fig. 5 shows typical thermal shutdown performance. When the junction temperature of the IC exceeds 150°C the bottom drives are disabled (see Fig. 5). When the IC temperature drops below 135°C the output is enabled again.

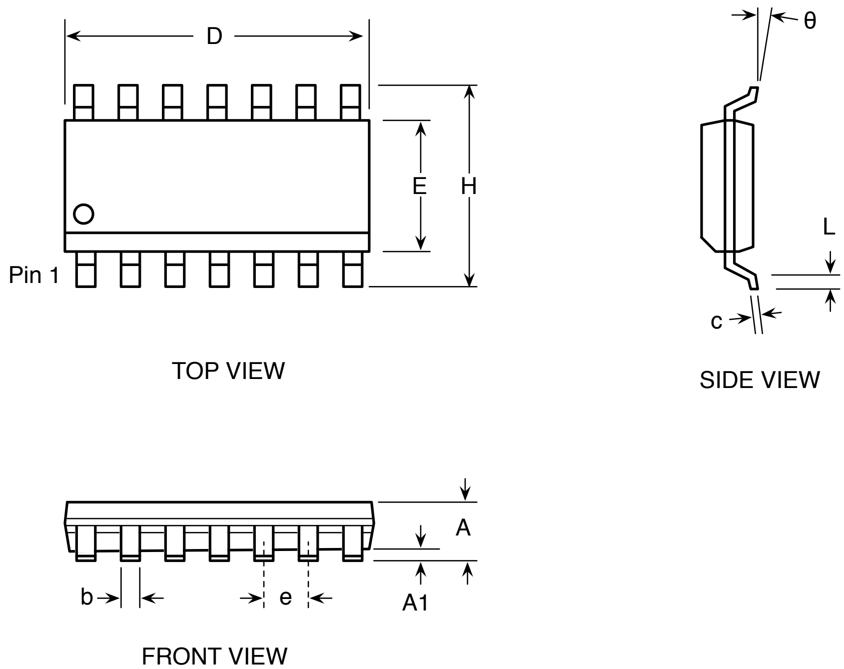
Current Limit

Motor current is sensed at the bottom of the H-Bridge across a resistor between the CLIM (Current LIMit) pin and ground. If this voltage exceeds 200mV, the bottom drives are disabled. The current limit comparator has 20mV of hysteresis.

Under Voltage

Upon power up, the Under Voltage block disables the bottom side pre-drivers until the voltage on VDD is sufficient to guarantee proper operation. In addition internal 20kΩ pulldown resistors in parallel with the bottom side pre-drivers guarantee the H-Bridge is turned off when the IC has no power and when power is first applied. Fig. 6 shows typical under voltage hysteresis. With VDD increasing, the pre-drivers are enabled at 4.7V and disabled when VDD drops below 4.2V.

PACKAGE DRAWINGS



SYMBOL	Inches		Millimeters	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
b	0.013	0.020	0.33	0.51
c	0.008	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
θ	0°	8°	0°	8°
Note: controlling dimensions are in inches.				

Fig.16: SO14N, 14 Pin Narrow SOIC Package Outline